MP2460

45V, 0.6A, 1.7MHz, Synchronous Step-Down Converter in a TSOT23-6 Package

DESCRIPTION

The MP2460 is a high-frequency, step-down switching converter with integrated high-side and low-side power MOSFETs. The device can provide up to 0.6A of output current with current mode control for fast loop response.

The device's wide 4.5V to 45V input voltage range accommodates a variety of step-down applications, and the 1μA shutdown mode quiescent current allows the device to be used in battery-powered applications. The MP2460 uses a high duty cycle and low-dropout mode when the input voltage is low.

The MP2460 achieves high power conversion efficiency across a wide load range by scaling down the switching frequency under light-load conditions. This reduces switching and gate driving losses.

The MP2460 has built-in protection features, such as cycle-by-cycle current limiting, short-circuit protection (SCP) with hiccup mode, and thermal shutdown in the event of excessive power dissipation.

The MP2460 is available in a TSOT23-6 package.

FEATURES

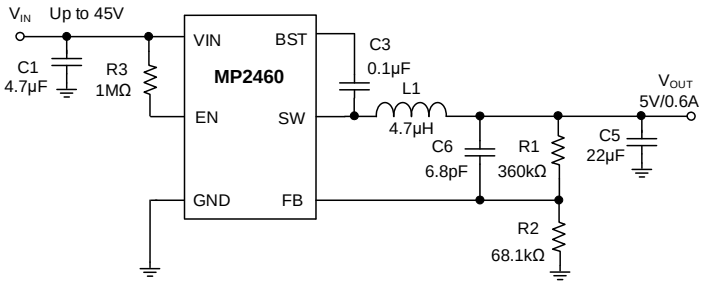
- Low-Dropout Mode
- Wide 4.5V to 45V Operating Input Range
- 98% Maximum Duty Cycle
- Light-Load Mode
- Dedicated Internal Compensation
- Stable with Ceramic and Electrolytic Output Capacitors
- 420mΩ/220mΩ Internal Power MOSFETs
- 1.7MHz Fixed Switching Frequency
- Internal Soft Start (SS)
- Precision Current Limit without a Current-Sense Resistor
- Meets 0.1% Output Voltage Ripple with Output Electrolytic Capacitor
- Short-Circuit Protection (SCP) with Hiccup Mode
- Output Adjustable from 0.8V to 0.98 x V_{IN}
- Over-Temperature Protection (OTP)
- Available in a TSOT23-6 Package

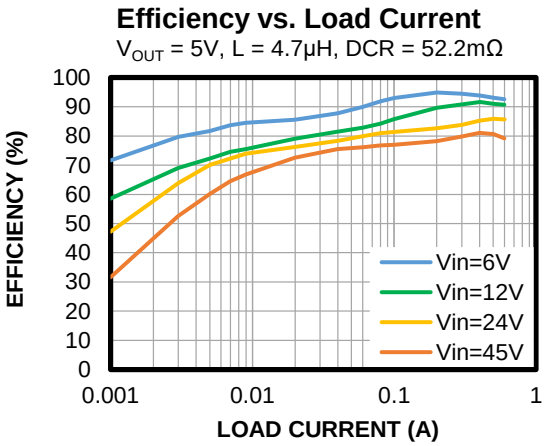
MPL Optimized Performance with MPS Inductor MPL-AL4020 Series, MPL-AL5050 Series, and MPL-SE6040 Series

APPLICATIONS

- Power Meters
- Aftermarket Automotive
- Multi-Function Printers (MFPs)
- General 36V Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2460GJ	TSOT23-6	*See Below*	1

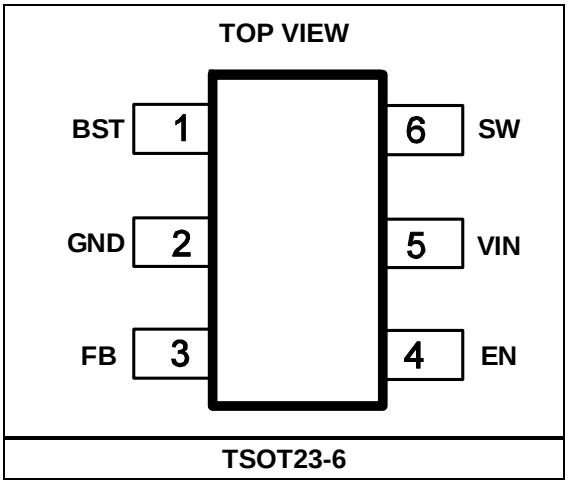
* For Tape & Reel, add suffix -Z (e.g. MP2460GJ-Z).

TOP MARKING

BPQY

BPQ: Product code of MP2460GJ
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** BST is the positive power supply for the internal, floating, high-side MOSFET driver. Connect a bypass capacitor between BST and SW.
2	GND	**Ground.** Connect an output capacitor as close to GND as possible. Avoid routing GND near high-current switch paths.
3	FB	**Feedback.** FB is the error amplifier input. Connect FB to an external resistor divider between the output and GND. Compare FB to the internal 0.8V reference to set the regulation voltage.
4	EN	**Enable input.** Pull EN below the specified threshold to shut the chip down. Pull EN above the specified threshold to enable the chip. Float EN to disable the chip.
5	VIN	**Input supply.** VIN supplies power to the internal control circuitry, both BST regulators, and the high-side switch. To reduce switching spikes, place a decoupling capacitor from VIN to ground, as close as possible to VIN.
6	SW	**Switch node.** The SW pin is the converter's switching output. SW is internally connected to the source of the high-side FET and the drain of the low-side FET. Connect SW to a power inductor.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to +48V
Switch voltage (V_{SW})…… ..-0.6V (-5V in 10ns) to V_{IN} + 0.3V (50V in 10ns)
BST to SW .....-0.3 to +6.0V
All other pins..... -0.3V to +6.0V (2)
EN Current.....100µA (2)
Continuous power dissipation (T_A = 25°C) (3) (5) 1.69W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM) .....±2000V
Charged device model (CDM) .....±750V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 4.5V to 45V
Output voltage (V_{OUT}).....0.8V to 0.98 x V_{IN}
EN current .....<50µA (2)
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

TSOT23-6			
EVL2460-J-00A (5)	74	24	°C/W
JESD51-7 (6)	100	55	°C/W

Notes:

1) Exceeding these ratings may damage the device. The value of V_{IN} is guaranteed at T_J = 25°C.
2) For details on the EN pin's absolute maximum rating, please see the Enable (EN) Control section on page 14.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EVL2460-J-00A, 2-layer PCB, 50.8mmx50.8mm.
6) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. The values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_{EN} = 2V, T_J = -40°C to +125°C [7], typical values at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback voltage	V_{FB}	T_J = -40°C to +125°C	0.78	0.8	0.82	V
		T_J = 25°C	0.788	0.8	0.812	
Feedback leakage	I_{LK_FB}	V_{EN} = 1V, V_{FB} = 2V			0.1	µA
High-side switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		420		mΩ
Low-side switch on resistance	R_{ON_LS}	V_{IN} = 15V		220		mΩ
High-side switch leakage	LKG_{HS}	V_{EN} = 0V, V_{SW} = 0V			1	µA
Low-side switch leakage	LKG_{LS}	V_{EN} = 0V, V_{SW} = 45V			1	µA
High-side current limit	I_{LIM_HS}			1.25		A
Low-side current limit	I_{LIM_LS}		0.7	0.9	1.1	A
V_{IN} UVLO rising threshold	VIN_{UVR}		4.1	4.3	4.5	V
V_{IN} UVLO falling threshold	VIN_{UVF}		3.75	4.0	4.25	V
V_{IN} UVLO hysteresis	VIN_{UV_HYS}			0.3		V
Soft-start time	t_{SS}	V_{FB} from 10% to 90%	0.35	0.6	0.85	ms
Oscillator frequency	f_{SW}		1.39	1.7	2.04	MHz
Minimum switch on time [8]	t_{ON_MIN}			100		ns
Maximum switch on time [8]	t_{ON_MAX}			5.2		µs
Minimum switch off time [8]	t_{OFF_MIN}			92		ns
Shutdown supply current	I_{QS}	V_{EN} < 0.3V, V_{IN} = 15V		1	2	µA
Quiescent supply current	I_Q	No load, V_{FB} = 0.83V, no switching		150	220	µA
Thermal shutdown [8]	T_{SD}			151		°C
Thermal shutdown hysteresis [8]	T_{SD_HYS}			21		°C
Enable rising threshold	V_{EN_R}	Low to high	1.5	1.55	1.6	V
Enable falling threshold	V_{EN_F}	High to low	1.1	1.22	1.3	V
Enable threshold hysteresis	V_{EN_HYS}			330		mV

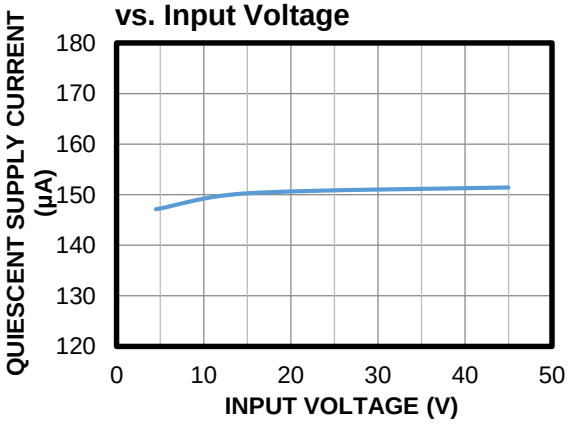
Notes:

7) Not tested in production. Derived by over-temperature correlation.
8) Not tested in production. Derived from bench characterization.

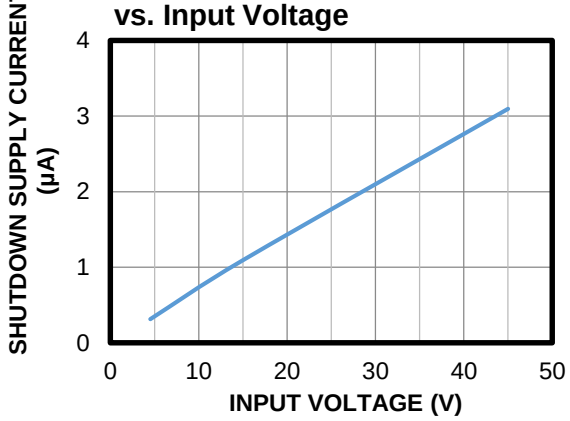
TYPICAL CHARACTERISTICS

V_{IN} = 15V, T_A = 25°C, unless otherwise noted.

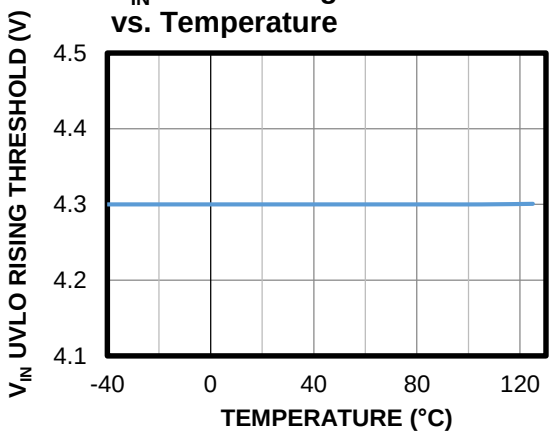
Quiescent Supply Current vs. Input Voltage



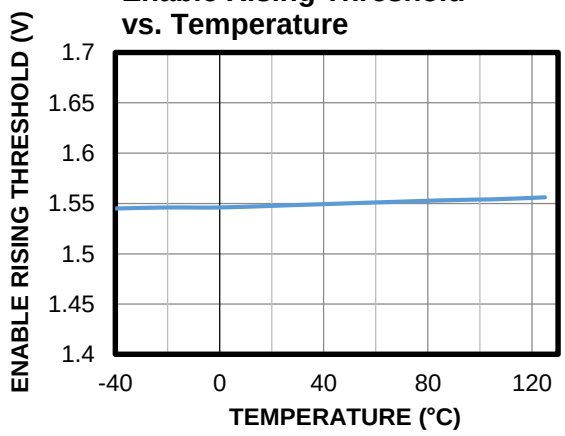
Shutdown Supply Current vs. Input Voltage



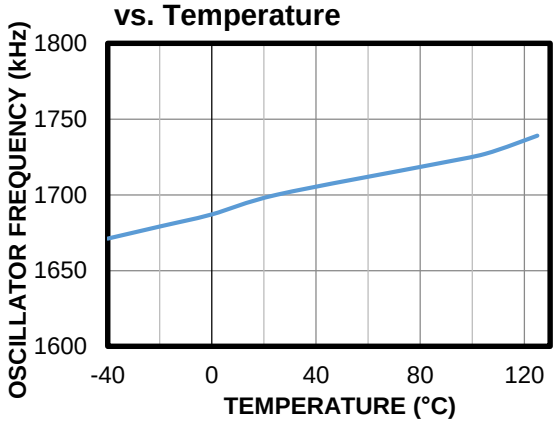
V_{IN} UVLO Rising Threshold vs. Temperature



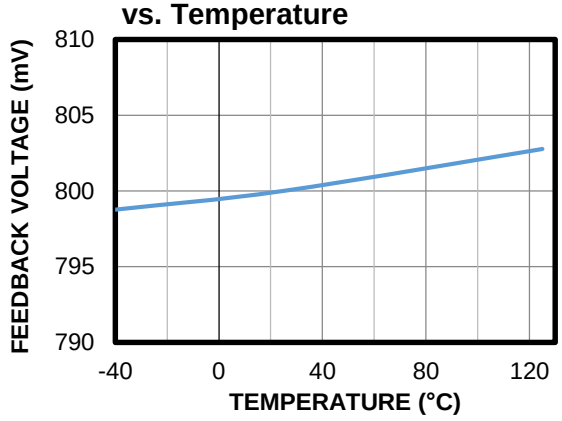
Enable Rising Threshold vs. Temperature



Oscillator Frequency vs. Temperature



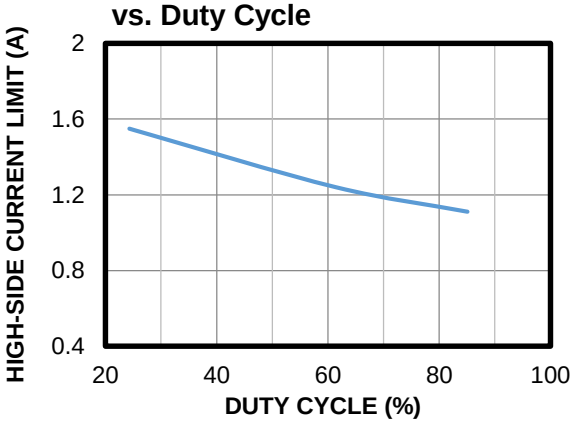
Feedback Voltage vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 15V, T_A = 25°C, unless otherwise noted.

High-Side Current Limit vs. Duty Cycle

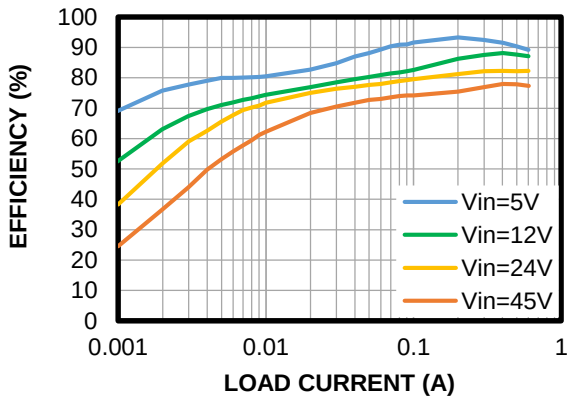


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section on page 18. V_{IN} = 24V, V_{OUT} = 5V, C1 = 4.7µF, C5 = 22µF, L1 = 4.7µH, and T_A = 25°C, unless otherwise noted.

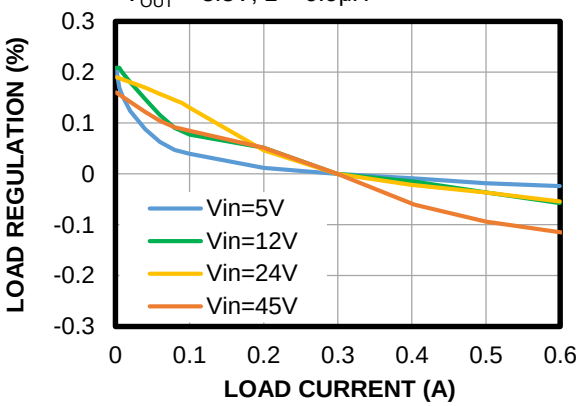
Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 3.3µH, DCR = 34.5mΩ



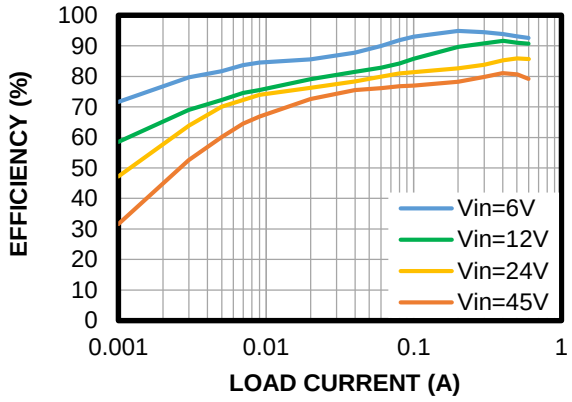
Load Regulation

V_{OUT} = 3.3V, L = 3.3µH



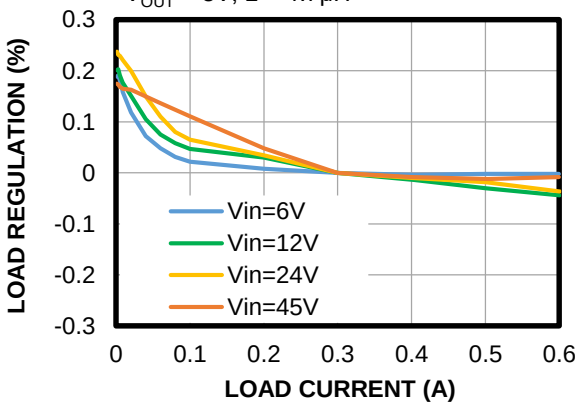
Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, DCR = 52.2mΩ



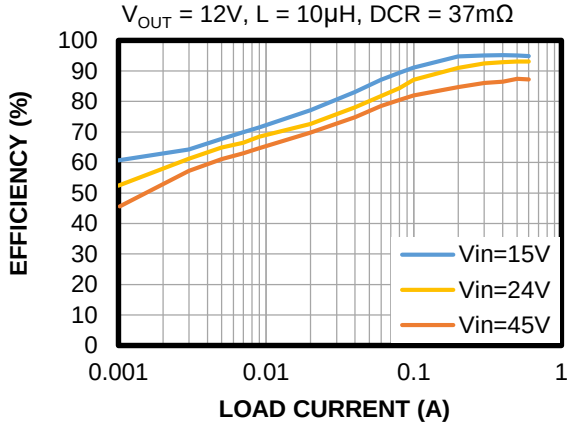
Load Regulation

V_{OUT} = 5V, L = 4.7µH



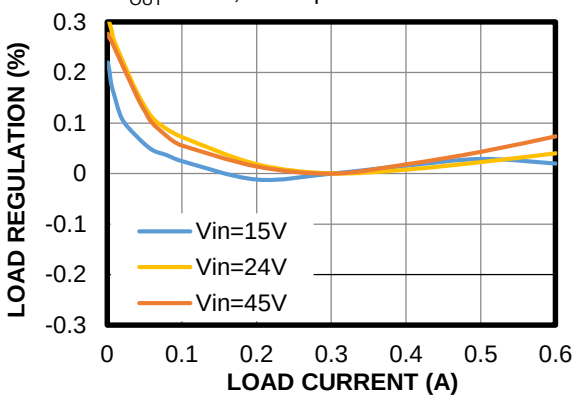
Efficiency vs. Load Current

V_{OUT} = 12V, L = 10µH, DCR = 37mΩ



Load Regulation

V_{OUT} = 12V, L = 10µH

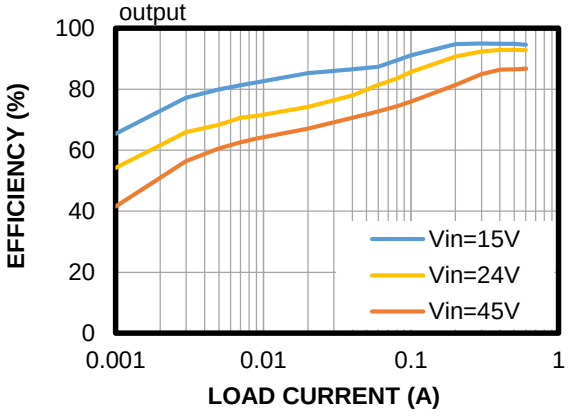


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 18. V_{IN} = 24V, V_{OUT} = 5V, C1 = 4.7µF, C5 = 22µF, L1 = 4.7µH, and T_A = 25°C, unless otherwise noted.

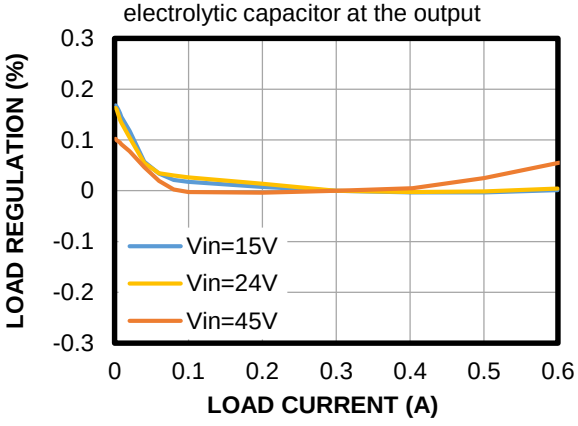
Efficiency vs. Load Current

V_{OUT} = 12V, L = 22µH, DCR = 97mΩ, add a 470µF electrolytic capacitor at the output

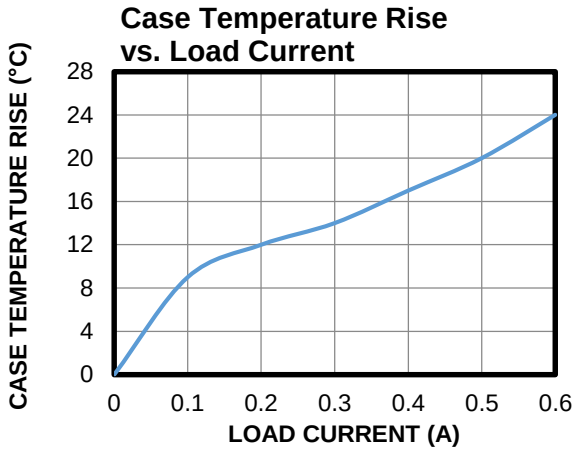


Load Regulation

V_{OUT} = 12V, L = 22µH, add a 470µF electrolytic capacitor at the output

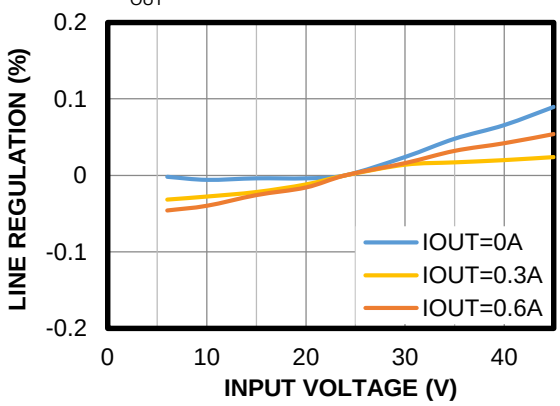


Case Temperature Rise vs. Load Current



Line Regulation

V_{OUT} = 5V

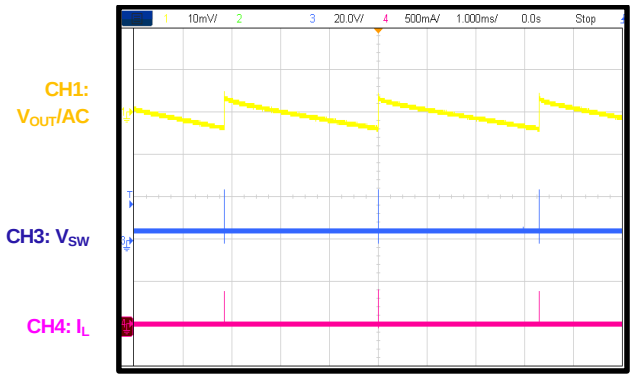


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 18. V_{IN} = 24V, V_{OUT} = 5V, C1 = 4.7µF, C5 = 22µF, L1 = 4.7µH, and T_A = 25°C, unless otherwise noted.

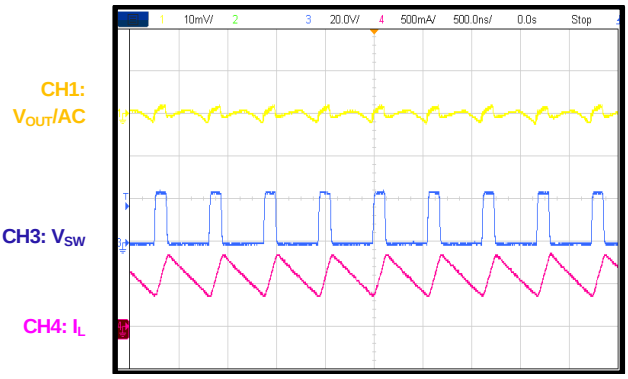
Steady State

I_{OUT} = 0A



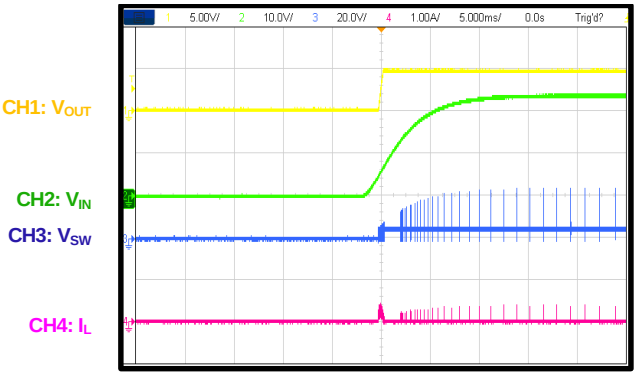
Steady State

I_{OUT} = 0.6A



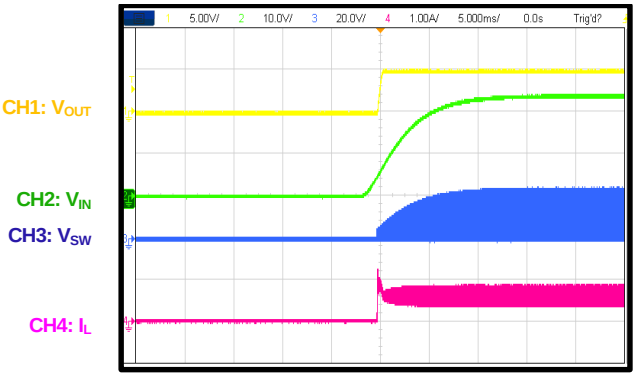
Start-Up through VIN

I_{OUT} = 0A



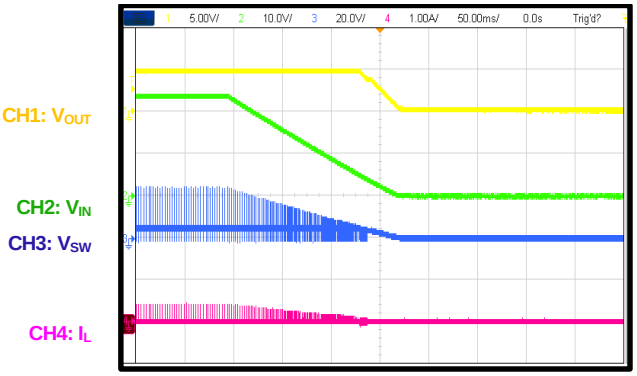
Start-Up through VIN

I_{OUT} = 0.6A



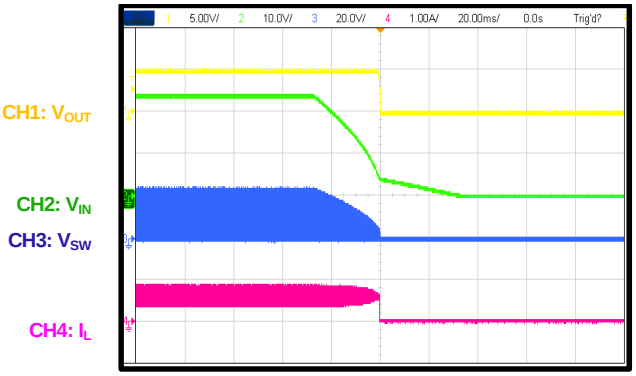
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 0.6A

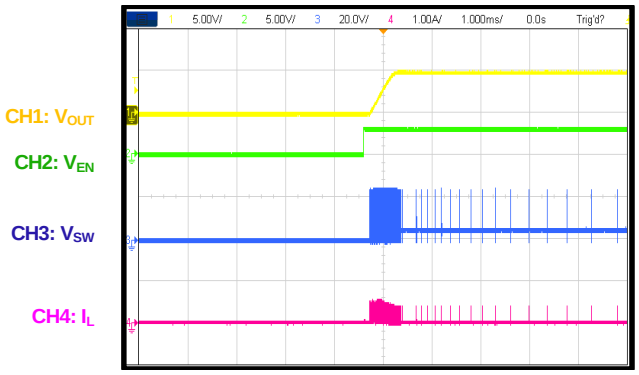


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 18. V_{IN} = 24V, V_{OUT} = 5V, C1 = 4.7µF, C5 = 22µF, L1 = 4.7µH, and T_A = 25°C, unless otherwise noted.

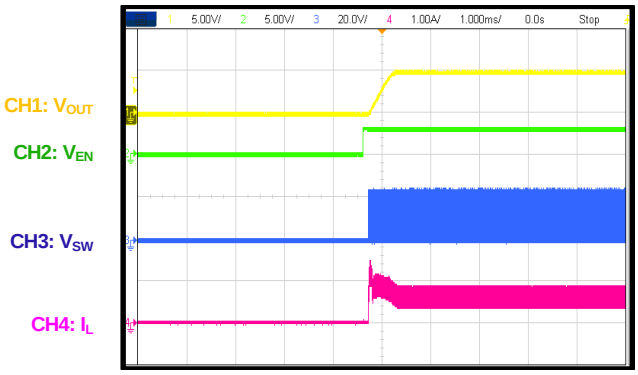
Start-Up through EN

I_{OUT} = 0A



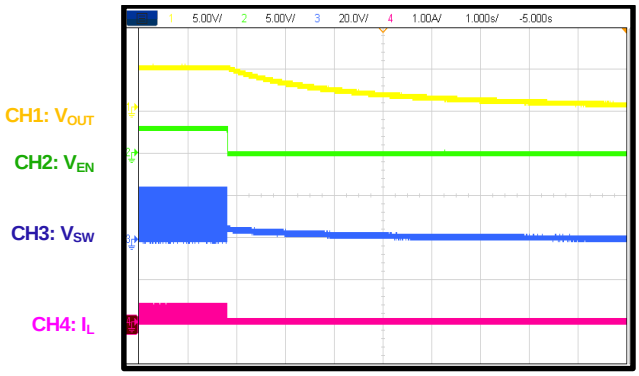
Start-Up through EN

I_{OUT} = 0.6A



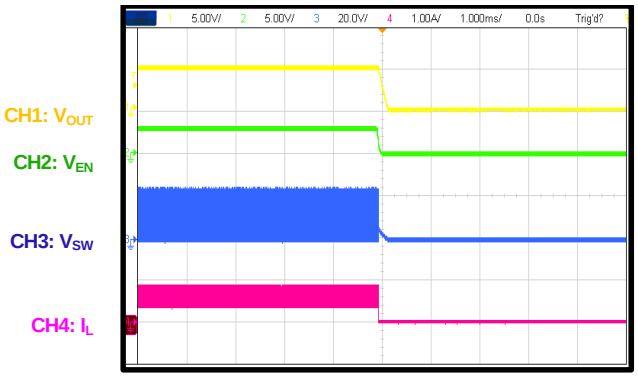
Shutdown through EN

I_{OUT} = 0A



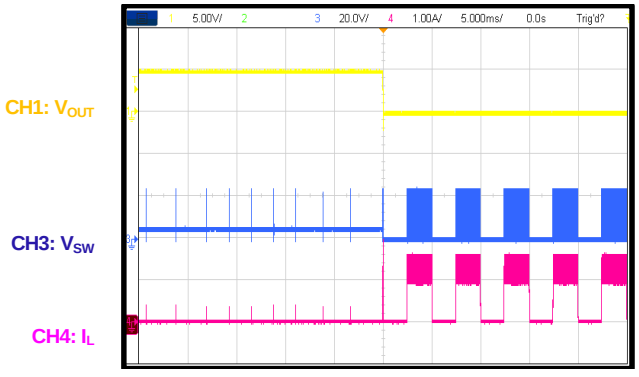
Shutdown through EN

I_{OUT} = 0.6A



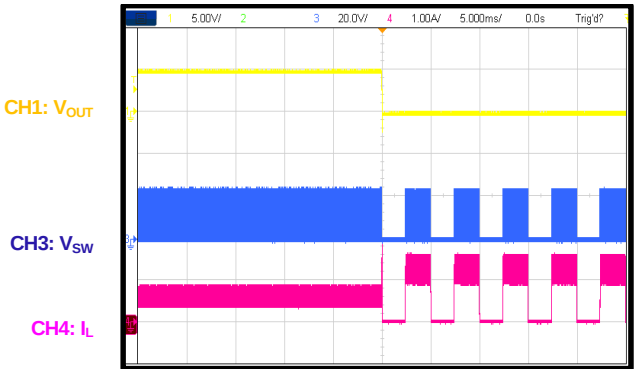
Short-Circuit Protection Entry

I_{OUT} = 0A



Short-Circuit Protection Entry

I_{OUT} = 0.6A

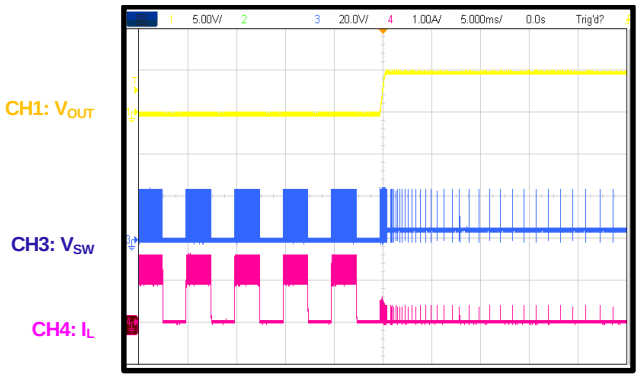


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 18. V_{IN} = 24V, V_{OUT} = 5V, C1 = 4.7µF, C5 = 22µF, L1 = 4.7µH, and T_A = 25°C, unless otherwise noted.

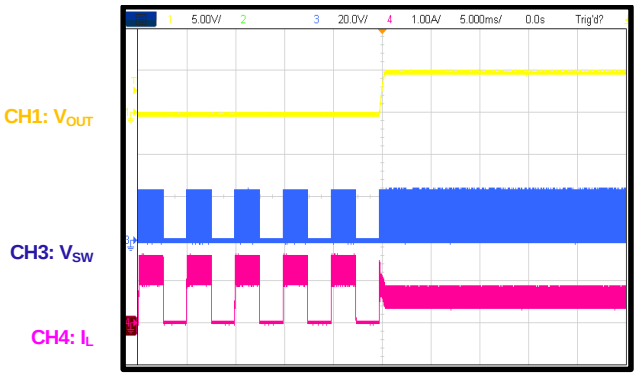
Short-Circuit Protection Recovery

I_{OUT} = 0A



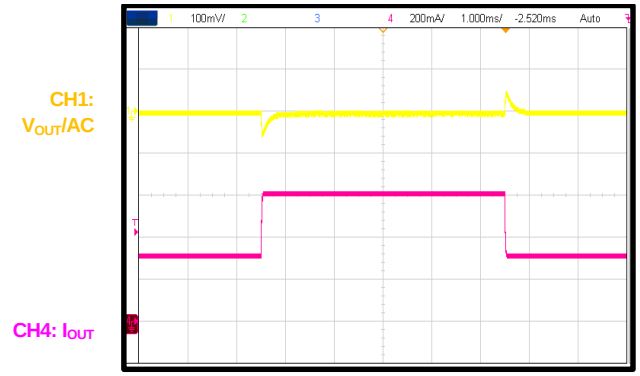
Short-Circuit Protection Recovery

I_{OUT} = 0.6A



Load Transient

I_{OUT} = 0.3A to 0.6A, 100mA/µs



FUNCTIONAL BLOCK DIAGRAM

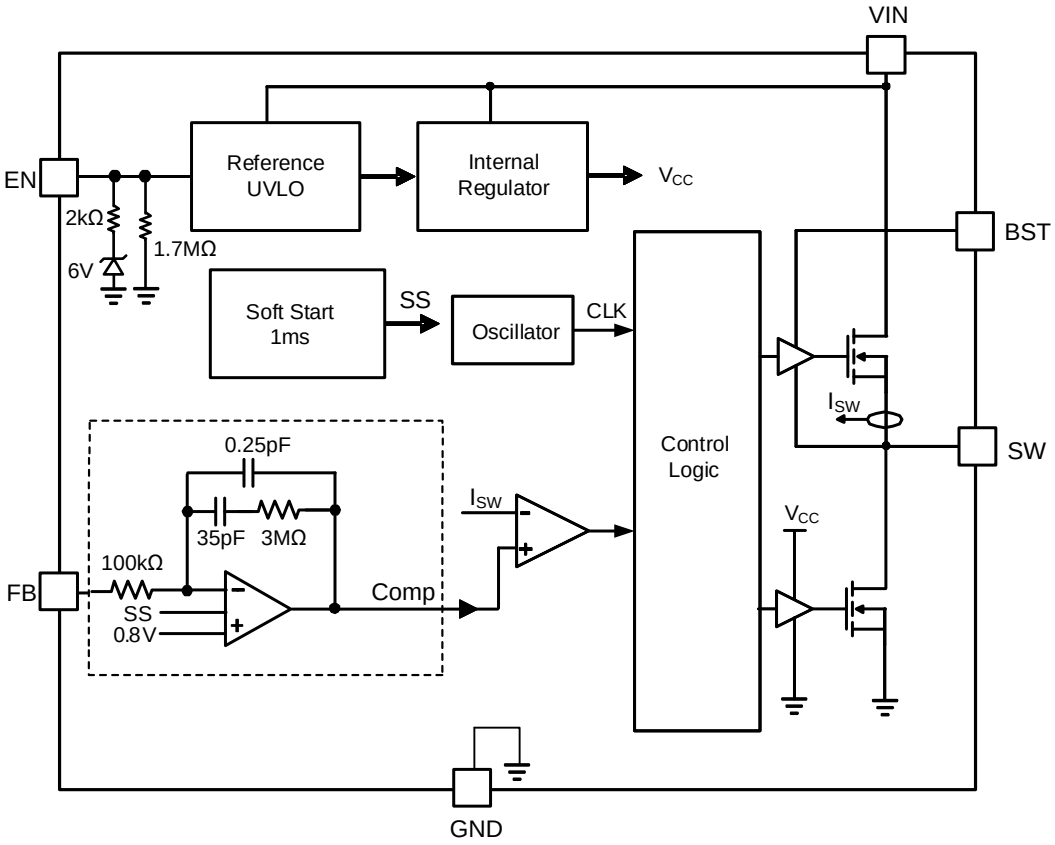


Figure 1: Functional Block Diagram

OPERATION

The MP2460 is a 1.7MHz, synchronous, step-down switching converter with integrated high-side and low-side power MOSFETs. The MP2460 provides an internally compensated, highly efficient output of up to 0.6A with current mode control. The device also features a wide input voltage range, internal soft-start control, and a precision current limit. Its very low operational quiescent current makes it well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MP2460 operates in a fixed-frequency, peak current control mode to regulate the output voltage. A pulse-width modulation (PWM) cycle initiated by the internal clock turns on the high-side MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}).

When the HS-FET turns off, the low-side MOSFET (LS-FET) turns on, and the inductor current flows through the LS-FET. To avoid shoot-though, a dead time is inserted to prevent the HS-FET and LS-FET from turning on at the same time. For each switching cycle, the HS-FET turns on and off with a minimum on and off time.

To prevent inductor current and output voltage runaway, the switching frequency folds back when the HS-FET minimum turn on time is detected internally.

When the PWM signal goes low, the HS-FET turns off and remains off for at least the minimum switch off time (t_{OFF_MIN}) before the next cycle begins. If the current in the HS-FET does not reach the value set by COMP within one PWM cycle, the HS-FET remains on to avoid a turn-off operation.

Pulse-Skip Mode (PSM)

Under light-load conditions, the MP2460 enters pulse-skip mode (PSM) to improve efficiency. PSM is triggered when V_{COMP} drops below the internal sleep threshold, which generates a pause command to block the turn-on clock pulse, so the power MOSFET does not turn on. This reduces gate driving and switching losses. The pause command causes the entire chip to enter sleep mode, which reduces the quiescent current to improve light-load efficiency.

When V_{COMP} exceeds the sleep threshold, the pause signal resets, and the chip resumes normal PWM operation. When the pause command changes from low to high, the PWM signal goes high immediately and turns on the power MOSFET.

Error Amplifier (EA)

The error amplifier is composed of an internal operational amplifier with an RC feedback network connected between its output node (internal COMP node) and its negative input node (FB). When the FB voltage (V_{FB}) drops below the internal reference voltage (V_{REF}), the operational amplifier drives the COMP output high, producing a higher switch peak current output and delivering more energy to the output. Conversely, when V_{FB} rises, the switch peak current output drops.

Connect FB to the tap of a voltage divider (R_1 and R_2), which is connected between the output and GND. In addition to the internal compensation RC network, R_1 also controls the error amplifier gain.

Enable (EN) Control

The MP2460 has a dedicated enable (EN) control pin. When V_{IN} rises above the threshold, EN can enable or disable the chip for high effective logic. An internal resistor from EN to GND allows EN to be floated to shut down the IC.

EN is clamped internally using a 6V series Zener diode (see Figure 2). Connect the EN input to VIN through a pull-up resistor to limit the EN input current below 50μA. For example, if 12V is connected to VIN, R_{PULLUP} ≥ (12V - 6V) / 50μA = 120kΩ.

If EN is connected directly to a voltage source without a pull-up resistor, limit the voltage source ≤6V to prevent damage to the Zener diode.

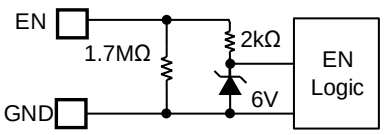


Figure 2: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

V_{IN} under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. For the UVLO rising and falling thresholds, see the Electrical Characteristics section on page 5.

Internal Soft Start (SS)

Soft start (SS) prevents the output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1V during the SS time. When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF} as the error amplifier reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

When the MP2460 starts up with a large output capacitor, the IC current limit may be triggered, which limits the output voltage rising slew rate. To avoid falsely triggering hiccup protection in this scenario, the MP2460 automatically extends the internal soft-start time.

Thermal Shutdown

Thermal shutdown prevents thermal runaway. When the silicon die temperature exceeds its upper threshold, the entire chip shuts down. When the temperature drops below its lower threshold, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection.

The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes falls below regulation, a P-channel MOSFET pass transistor connected from VIN to BST turns on. The charging current path goes from VIN to BST to SW. The external circuit must provide enough voltage headroom to facilitate the charging.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP2460 has both valley current limit control and peak current limit control.

During the LS-FET on period, the inductor current is monitored. When the sensed inductor current exceeds the valley current limit threshold, over-current protection (OCP) is triggered. The HS-FET does not turn on until the inductor current drops below the valley current limit.

During the HS-FET on period, the inductor current is sensed and compared to the peak current limit. If the peak current limit is triggered, the on pulse is terminated immediately.

The output voltage drops until V_{FB} falls below the under voltage (UV) threshold (typically 50% below the reference). Once a UV condition is triggered, the MP2460 enters hiccup mode to periodically restart the part.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft-start capacitor, and attempts to soft start again automatically. If the over-current condition remains after soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

Low-Dropout Operation

The MP2460 automatically raises the frequency to support applications where V_{IN} is close to V_{OUT}. The frequency extension circuit is triggered after t_{OFF_MIN} is reached. The MP2460 can support up to a 98% maximum duty cycle.

Pre-Biased Start-Up

The MP2460 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft-start capacitor is charged as well. If the BST voltage exceeds its rising threshold voltage, and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

APPLICATION INFORMATION

Setting the Output Voltage

Set the output voltage (V_{OUT}) with a resistor divider (see Figure 3):

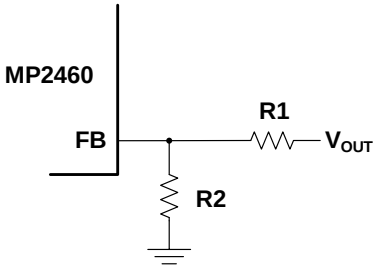


Figure 3: FB Resistor Divider to Set V_{OUT}

Calculate V_{OUT} with Equation (1):

$$V_{OUT} = V_{FB} \frac{(R1+R2)}{R2} \quad (1)$$

The feedback resistor (R1) also sets the feedback loop bandwidth with the internal compensation network.

To achieve optimal stability and transient response, choose R1 to be about 360kΩ in applications with a 5V output rail. R2 can be estimated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1} \quad (2)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection vs. Output Voltage Setting

V_{OUT}	R1	R2
3.3V	360kΩ (1%)	115kΩ (1%)
5V	360kΩ (1%)	68.1kΩ (1%)
12V	360kΩ (1%)	25.5kΩ (1%)
12V (9)	150kΩ (1%)	10.7kΩ (1%)

Note:

9) Add a 470µF electrolytic and use a 22µH inductor to achieve a 0.1% output voltage ripple for power meter applications.

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AL4020 Series, MPL-AL5050 Series, and MPL-SE6040 Series**

The inductor supplies constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current.

To determine the inductance, allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. Choose a peak inductor current below the maximum switch current limit. With low-ESR output capacitors (e.g. MLCC), make the inductor current ripple about 60% to 100% of the maximum load current to further reduce the inductor size and power loss. The inductance can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_{SW} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Where I_{OUT} is the load current.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AL4020-3R3	3.3µH	MPS
MPL-AL4020-4R7	4.7µH	MPS
MPL-AL5050-100	10µH	MPS
MPL-SE6040-220	22µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

The input capacitor (C1) can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic capacitor (C2, about 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that there is enough capacitance to provide a sufficient charge and prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. Low-ESR capacitors are recommended to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (6)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

If using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

In power meter applications, larger-value capacitors are generally used as the output capacitors (C4). The capacitance and R_{ESR} for these capacitors fluctuate at lower temperatures. This large temperature variation changes the part's feedback loop, making it difficult to keep the loop stable across the full operation temperature range. It is recommended to use tantalum or polymer capacitors for low-temperature applications since they are more stable across wide temperature ranges.

Selecting Compensation Components

The goal of compensation design is to shape the converter's transfer function to set an optimal loop gain. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies can cause system instability. Generally, set the crossover frequency to be approximately one-tenth of the switching frequency. If using an electrolytic capacitor, select a loop bandwidth no higher than 1/4 of the ESR zero-frequency (f_{ESR}). f_{ESR} can be calculated with Equation (9):

$$f_{ESR} = \frac{1}{2\pi \times C4 \times R_{ESR}} \quad (9)$$

Table 3 shows a component selection guide for 12V, 5V, and 3.3V output rail applications.

Table 3: Components Selection Guide

V_{OUT}	R1	R2	C6	L1	C5	C4
3.3V	360kΩ (1%)	115kΩ (1%)	4.7pF	3.3µH	22µF	NS
5V	360kΩ (1%)	68.1kΩ (1%)	6.8pF	4.7µH	22µF	NS
12V	360kΩ (1%)	25.5kΩ (1%)	10pF	10µH	22µF	NS
12V (10) E-Cap	150kΩ (1%)	10.7kΩ (1%)	NS	22µH	22µF	470µF

Note:

10) Add a 470µF electrolytic capacitor and use a 22µH inductor to achieve a 0.1% output voltage ripple for power meter applications.

Design Example

Table 4 lists a design example following the application guidelines for the specifications below.

Table 4: Design Example

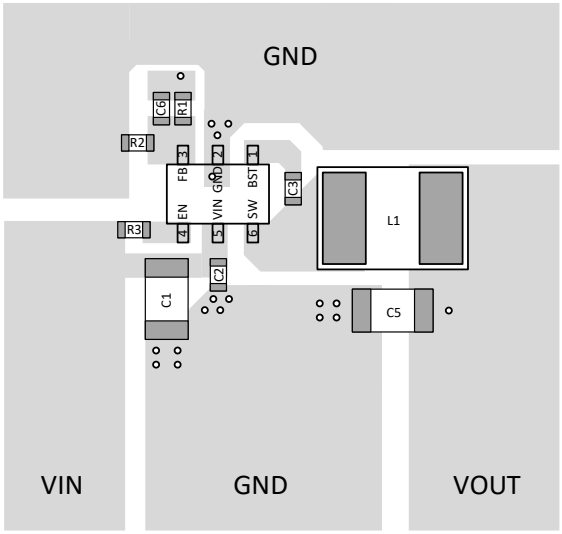
V_{IN}	24V
V_{OUT}	5V
f_{SW}	1.7MHz

Figure 6 on page 19 shows the detailed application schematic. For the typical performance and waveforms, see the Typical Performance Characteristic section on page 8. For more devices applications, refer to the related evaluation board datasheet.

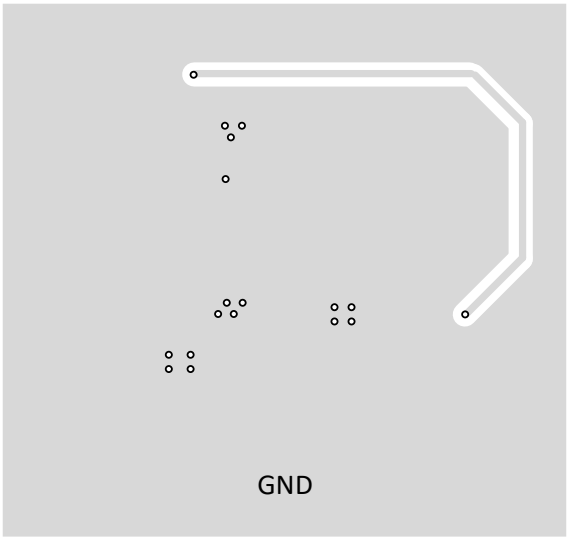
PCB Layout Guidelines

Efficient PCB layout requires high-frequency noise considerations to limit EMI noise and voltage spikes on the SW node. For the best results, refer to Figure 4 and follow the guidelines below:

1. Keep the path of the input decoupling capacitor, VIN, SW, and PGND as short as possible using short and wide traces.
2. Keep the external feedback resistors as close to the FB pin as possible.
3. Run the feedback trace far from the inductor, switching node (such as SW, BST) and noisy power traces. If possible, run the feedback trace on the opposite side of the PCB from the inductor, separated by a ground plane.
4. Add a grid of thermal vias under the exposed pad to improve thermal conductivity.
5. Use small vias (15mil barrel diameter) to fill the hole during the plating process. This also prevents solder wicking during the reflow process, which is associated with larger vias.
6. Use a pitch (distance between the centers) of approximately 40mil between the thermal vias.



Top Layer



Bottom Layer

Figure 4: Recommended Layout

TYPICAL APPLICATION CIRCUITS

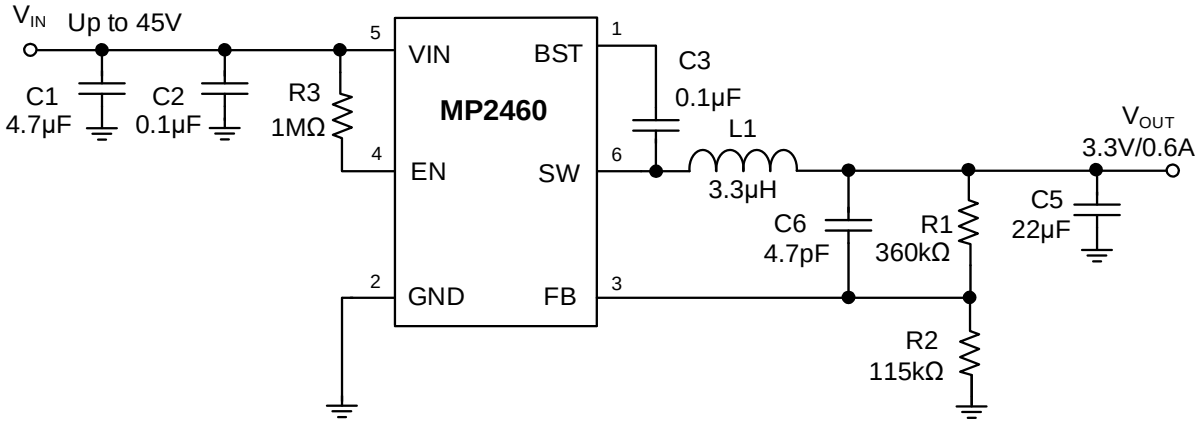


Figure 5: Typical Application Circuit (3.3V Output)

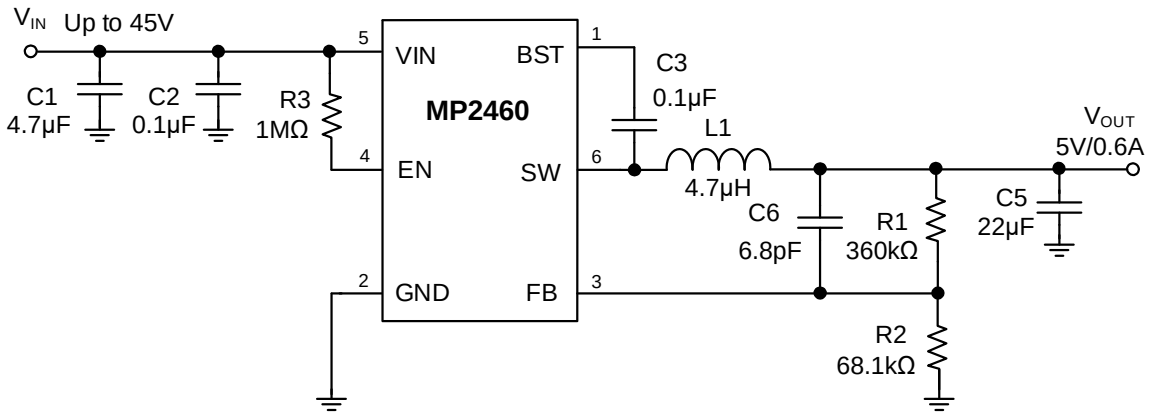


Figure 6: Typical Application Circuit (5V Output)

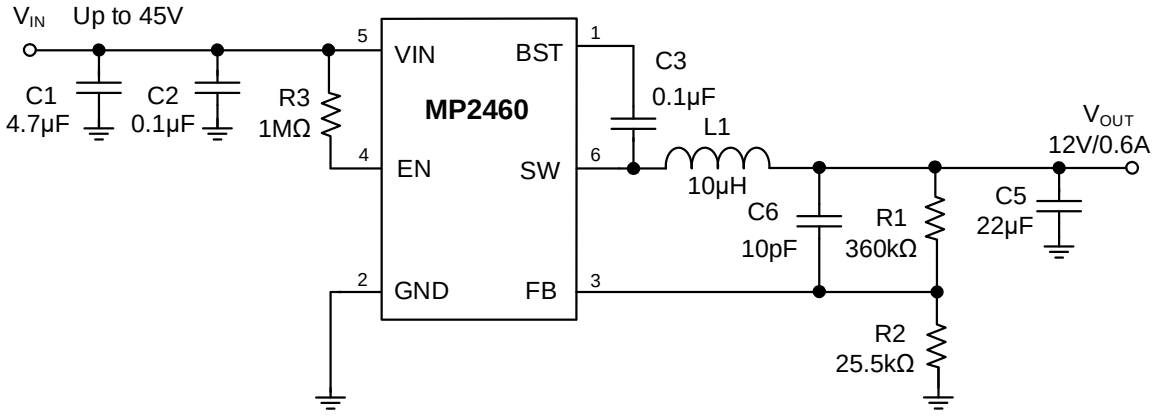


Figure 7: Typical Application Circuit (12V Output)

TYPICAL APPLICATION CIRCUITS *(continued)*

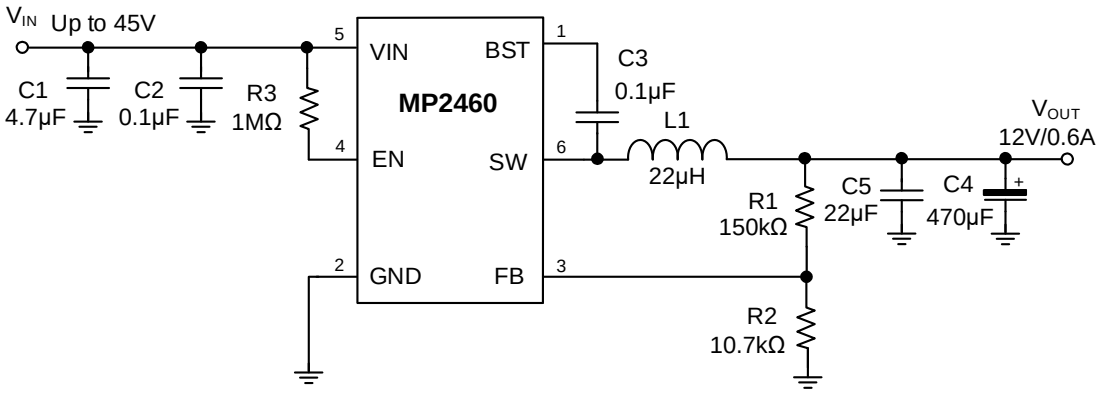


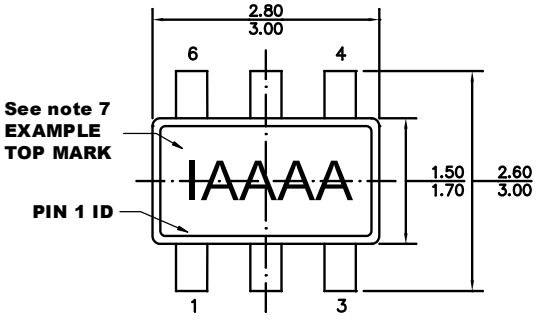
Figure 8: Typical Application Circuit (12V Output with Large Output Electrolytic Capacitor) (11)

Note:

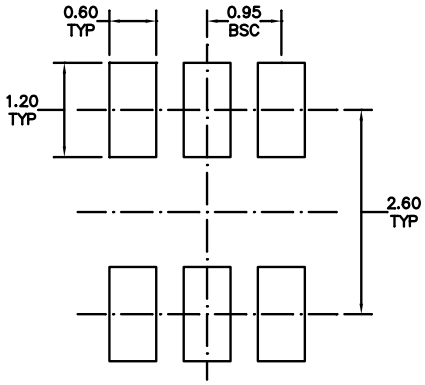
11) Add an electrolytic capacitor to achieve a 0.1% output voltage ripple for power meter applications.

PACKAGE INFORMATION

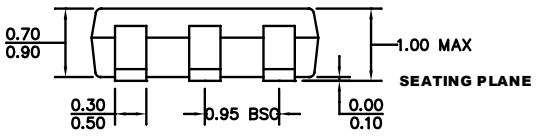
TSOT23-6



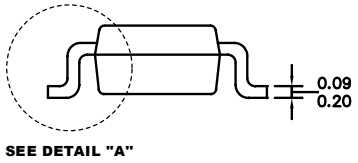
TOP VIEW



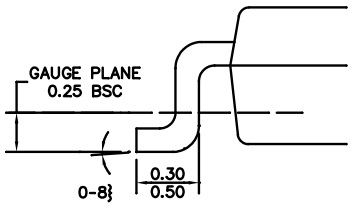
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

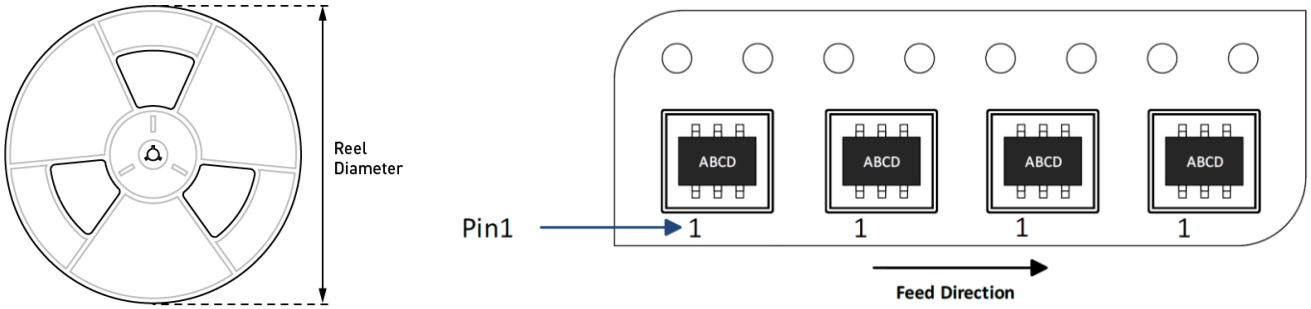


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2460GJ-Z	TSOT23-6	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/20/2021	Initial Release	-